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STUDY TO ESTABLISH CRITERIA FOR A SOLAR CELL ARRAY FOR USE AS A PRIMARY POWER SOURCE FOR A LUNAR-BASED WATER ELECTROLYSIS SYSTEM

PHASE IV - FINAL TECHNICAL REPORT

09681-6008-R000

15 SEPTEMBER 1971

CASE FILE
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Contract No. NAS 8-21189
Period covered: 15 December 1970 to 15 September 1971

Prepared for
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
George C. Marshall Space Flight Center
Huntsville, Alabama 35812

TRW
SYSTEMS GROUP

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15 December 1970 to 15 September 1971

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Lunar Surface Power System Project

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Prepared for:
National Aeronautics and Space Administration
George C. Marshall Space Flight Center
Huntsville, Alabama 35812
Contract No. NAS 8-21189

FOREWORD

This Phase IV - Final Technical Report for the "Study to Establish Criteria for a Solar Cell Array for Use as a Primary Power Source for a Lunar-Based Water Electrolysis System" was prepared for the National Aeronautics and Space Administration, George C. Marshall Space Flight Center, Huntsville, Alabama. This effort, together with that documented in the Phase I, II, and III Final Technical Reports (References 1.1, 1.2, and 1.3) completely fulfills the requirements of Contract NAS 8-21189. This report covers the lunar surface solar array development work performed from 15 December 1970 to 15 September 1971. It documents and summarizes the results of this program during this fiscal period.

This development work was conducted under the auspices of the Astrionics Laboratory, Power Systems Branch (Charles Graff-Chief) of NASA/MSFC. Technical direction was provided by James L. Miller (COTR). Distribution of this document is established by the Contracting Officer, Lawrence Garrison, or his authorized representative. Communications relative to this contract should be directed to the above Contract Specialist, Attention: Code PR-SC, George C. Marshall Space Flight Center, Huntsville, Alabama 35812.

ACKNOWLEDGEMENTS

This phase of the development program was conducted by the Electrical Systems Laboratory of the TRW Systems Group, which is under the direction of P.H. Greenler. The Project Manager and Principal Investigator was J.E. Boretz.

Acknowledgement is expressed to the various members of the TRW Systems Technical Staff named below for their assistance and valuable technical contribution to this phase of this development effort.

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R. F. Kennedy
G. R. Luckey
A. Robertshaw
B. N. Smith
T. J. Sereno
W. R. Wannlund
J. Yurk

In addition, the technical direction, guidance, reviews, and comments provided by J. L. Miller and other members of the NASA/MSFC Power Systems Branch (C. Graff, C. Kirby, J. Willis, and L. Crabtree) are also gratefully acknowledged.

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1. INTRODUCTION

1.1 GENERAL

This technical report encompasses the Phase IV development work that was performed under Contract NAS 8-21189. It represents the completion of this original technology program entitled, "Study to Establish Criteria for a Solar Cell Array for Use as a Primary Power Source for a Lunar-Based Water Electrolysis System", (References 1.1, 1.2 and 1.3). The work was carried out in accordance with the approved work statement of Reference 1.4. The report fulfills the contractual requirement for preparation of the Final Phase IV Report and covers the period from 15 December 1970 to 15 September 1971.

This overall program was initiated on 1 July 1967. Its original objective was to generate parametric data for large area solar arrays to be used for various lunar surface exploration missions. This work (Phase I) was completed on 30 June 1968 and reported in Reference 1.1. A follow-on effort was initiated at that time. This consisted of developing three prototype solar cell panel Engineering Test Models (ETM). These were baseline configurations suitable for use with a $45KM_e$ candidate lean-to solar array system. The three ETM's utilized various substrate materials (i.e., fiberglass lattice, Kapton, graphite composite) and a common, flat laydown cellstack configuration. They represented different degrees of technology refinement in the design of large area solar arrays and resulted in power-to-weight ratios of 12 to 18 watts per pound. This Phase II effort was completed on 15 November 1969 and reported in Reference 1.2.

During Phase III of this program, additional technology development work was conducted to evaluate a silicon cell spalling phenomenon which had occurred. This work consisted of analytically and experimentally evaluating the parameters associated with this cell degradation mode and resulted in establishing the cellstack material properties and design requirements for its elimination. The results of this work were reported in Reference 1.3.

The Phase IV effort was initiated to culminate the development effort on this program by selecting and qualifying a Prototype Engineering Test Model of a solar array panel. This would confirm the adequacy of the design and permit its use for future lunar surface applications.

1.2 PROGRAM OBJECTIVES

The overall objective of this program phase was to design and fabricate a prototype solar array panel based upon the new technology that had been developed. In addition, this panel was to be qualified by test to the launch, trans-lunar, and lunar surface environmental requirements as outlined in Reference 1.5. After evaluation of the qualification test data, a final solar array design was to be specified for use on future lunar surface missions. It was also desired that the new technology developed on this program could potentially provide solar array design criteria that would also be used for earth-orbital and planetary exploration missions as well.

1.3 PROGRAM APPROACH

The approach taken was to review the solar array module technology that had been developed on this program and select a substrate-cellstack combination that would comprise the Prototype ETM. This selected design, after review and approval by NASA/MSFC, was detailed and fabricated into the Prototype ETM. The Prototype ETM was shipped to NASA/MSFC for qualification testing in the Astrionics Laboratory Environmental Test Facility. Upon completion of these tests, the data was evaluated and a report was prepared summarizing the final design specifications for the prototype solar array panel.

2. SUMMARY

2.1 PROTOTYPE SOLAR ARRAY PANEL DESIGN

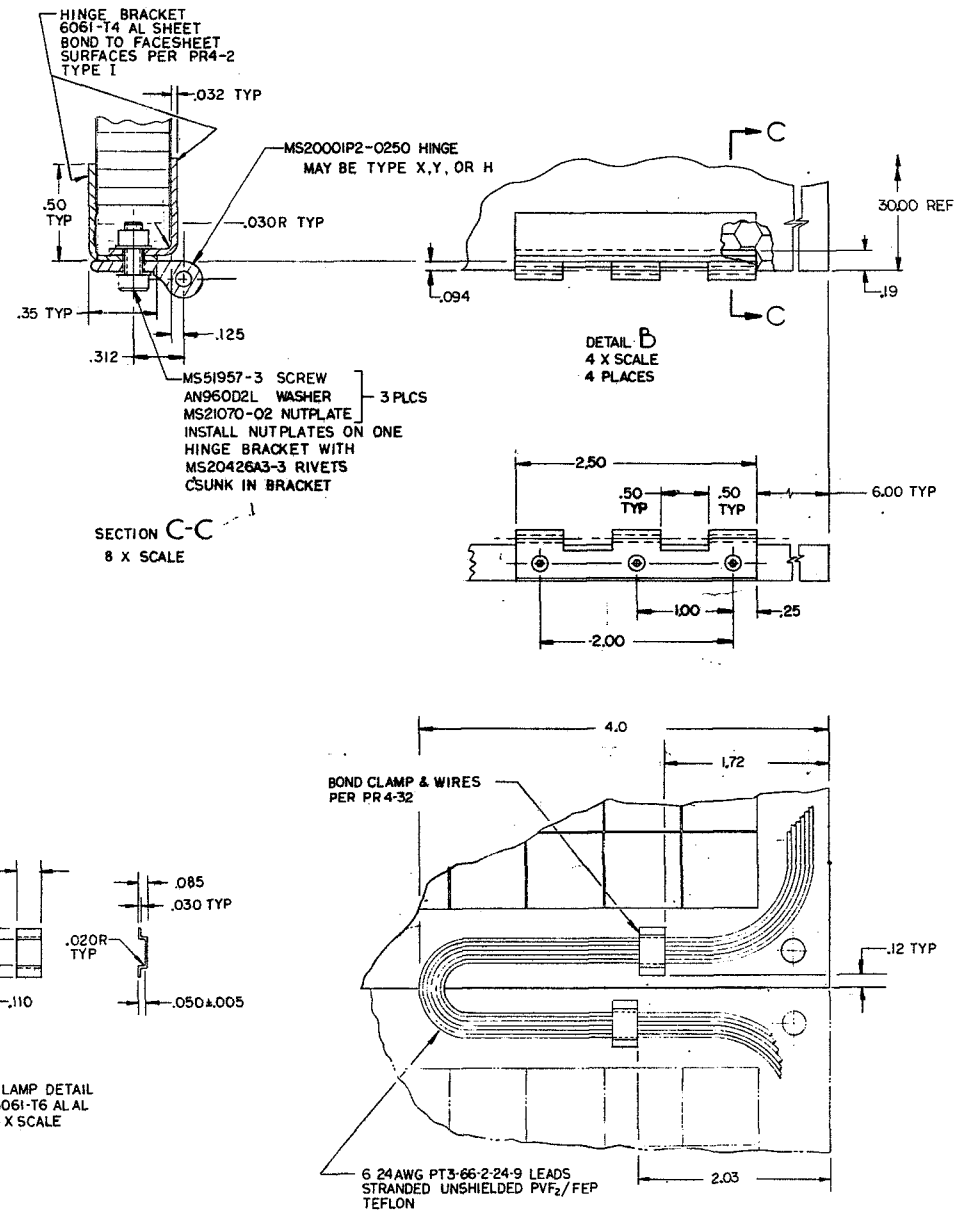
The main emphasis during this program phase was to design, fabricate and qualify a Prototype Test Module. The ETM III was selected as the prototype configuration. This was the module which employed the graphite composite face sheets on a light-weight aluminum honeycomb core to make up the substrate. The cellstack design was based upon the use of 2 cm x 4 cm silicon cells utilized in a flat laydown configuration.

The Prototype Test Module was a 30 inch x 48 inch panel. The final design configuration is shown on Figure 2.1. The cellstack consisted of seven strings, employing two cells in parallel and 66 cells in series, for a total of 924 cells. The detail of this design is shown on Figure 2.2. A summary of the major characteristics of the Prototype Test Module is provided in Table 2.1.

2.2 PROTOTYPE SOLAR ARRAY PANEL TESTING

The Prototype Solar Array panel was subjected to the structural-dynamic, acoustic, and thermal vacuum cycling tests as outlined in Reference 1.5. In addition, electrical performance tests were conducted at the beginning and upon completion of the qualification test program.

After the implementation of a minor modification to the support technique for the cell series string collector strips, the Prototype Solar Array panel successfully passed the qualification test program. This design configuration is now considered technology-ready for future lunar surface applications. In addition, because of its comparatively high specific power, it should also prove attractive for earth-orbital and planetary exploration programs where deployable, rigid panel solar arrays may be required.


HINGE BRACKET
6061-T4 AL SHEET
BOND TO FACESHEET
SURFACES PER PR4-2
TYPE I
.032 TYP
MS20001P2-0250 HINGE
MAY BE TYPE X,Y, OR H
.030R TYP
.50
TYP
.35 TYP
.125
.312
MS51957-3 SCREW
AN960D2L WASHER
MS21070-02 NUTPLATE
3 PLCS
INSTALL NUTPLATES ON ONE
HINGE BRACKET WITH
MS20426A3-3 RIVETS
CSUNK IN BRACKET
SECTION C-C
8 X SCALE
C
C
30.00 REF
.094
.19
DETAIL B
4 X SCALE
4 PLACES
2.50
.50
TYP
.50
TYP
6.00 TYP
1.00
.25
2.00
4.0
1.72
BOND CLAMP & WIRES
PER PR4-32
.12 TYP
2.03
6.24AWG PT3-66-2-24-9 LEADS
STRANDED UNSHIELDED PVF2/FEP
TEFLON
.250
.280
.500
.110
.085
.030 TYP
.020R
TYP
.050±.005
CLAMP DETAIL
6061-T6 AL AL
4 X SCALE
CONCEPT OF TYPICAL PANEL INTERCONNECT WIRING
4 X SCALE
INSTALL 2 HINGES AS SHOWN
INSTALL 2 OPPOSITE HINGES
AS SHOWN IN SECTION C-C
SECTION D-D
4 X SCALE
.030
6.24
1.60TYP
3.12
.070 TYP
.080 R. TYP
DETAIL OF LONG INTERCONNECT
KOVAR RIBBON .030 x .003
7 REQ.
.030
3.00
1.50
.070
.080 R.
DETAIL OF SHORT INTERCONNECT
KOVAR RIBBON .030 x .003
14 REQ.
SL603-4-400A INSERT
REF
FACE SHEET REF
CELL SIDE REF
HONEYCOMB CORE
.375
REF
.257 DIA HOLE
REF
SECTION A-A
4 X SCALE
14 PLACES
1.353
45.293 MAX.
1.386
P
N
27.228
MAX. REF.
30.00
3 EQUAL SPACES
= 29.250 BASIC
2 PLCS
N
P
.375
TYP
.375 TYP
4 EQUAL SPACES = 47.250 BASIC
2 PLACES
48.00
.686-.691 DIA
SL603-4-400A (SHURLOK CO)
ALTERNATE: FAB FROM ALUM ALY
PER SHURLOK CATALOG DIMS
INSTALL PER PROCEDURE OF
PR10-12 TYPE 1 CLASS 3
14 PLACES WITHIN .010 DIA TRUE POSITION
TOLERANCE EACH AT FINAL ASSY
MAIN VIEW
SHOWING DIMENSIONS AND
MOUNTING HOLE LOCATIONS

1

2

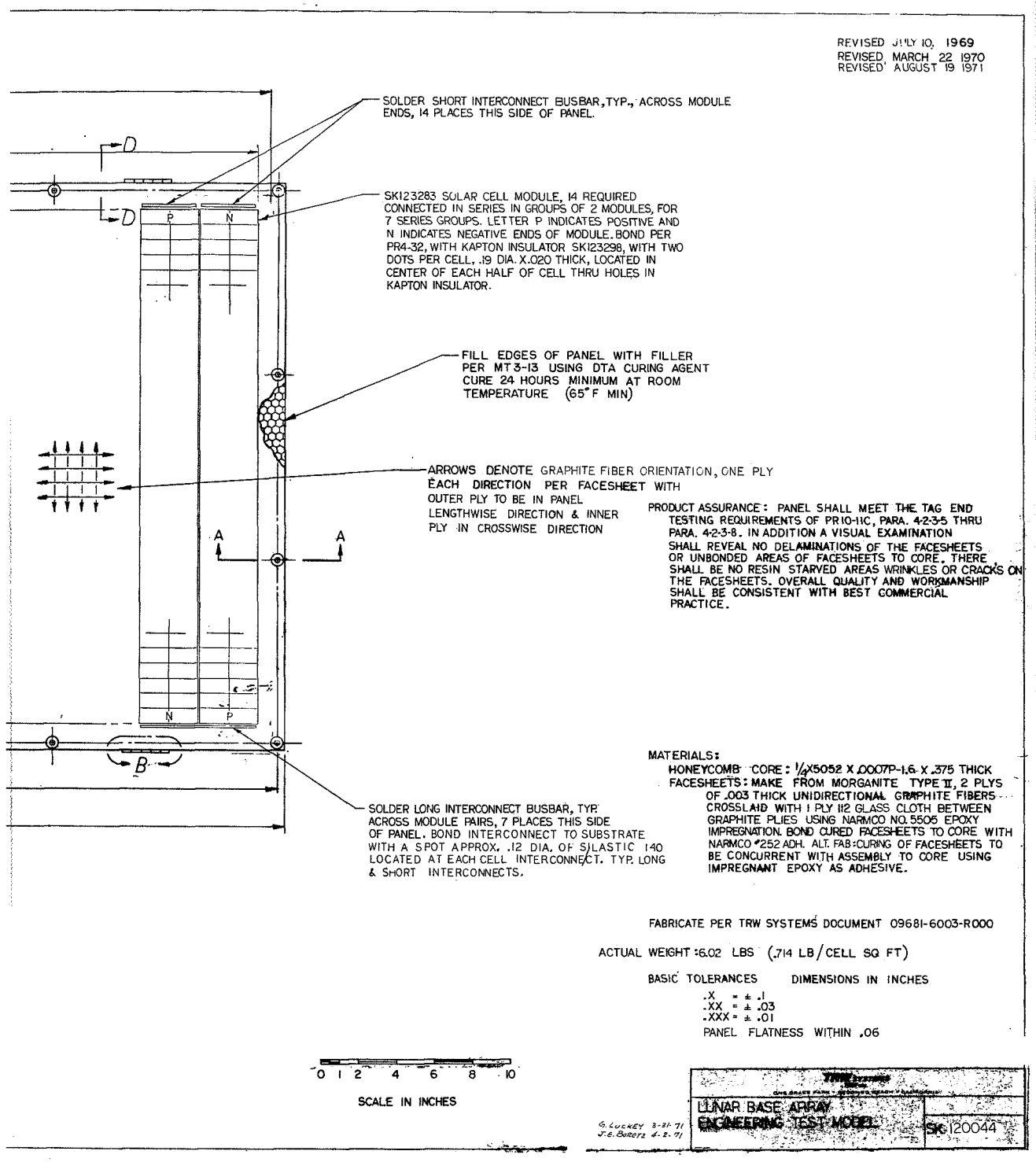
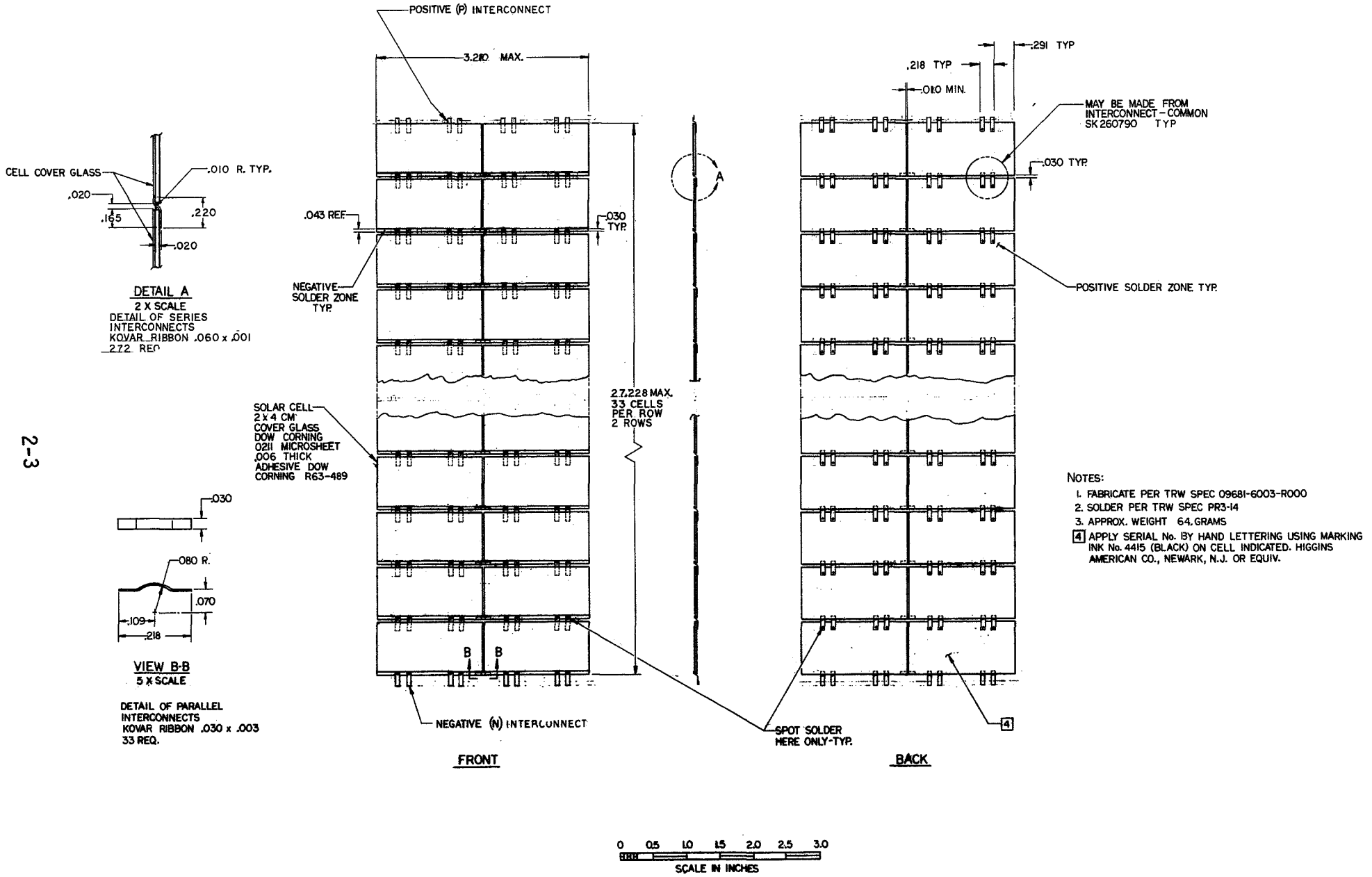


Figure 2.1 Prototype Test Module Assembly (ETM III Type)

3



NOTES:

1. FABRICATE PER TRW SPEC 09681-6003-R000
2. SOLDER PER TRW SPEC PR3-14
3. APPROX. WEIGHT 64. GRAMS
4. APPLY SERIAL No. BY HAND LETTERING USING MARKING INK No. 4415 (BLACK) ON CELL INDICATED. HIGGINS AMERICAN CO., NEWARK, N.J. OR EQUIV.

Figure 2.2 Prototype Test Module-Solar Cell Sub-Module Arrangement

TABLE 2.1

PROTOTYPE TEST MODULE DESIGN CHARACTERISTICS

Substrate	
° Face Sheets	Morganite Type II; 2 plys of 0.003 in. thick unidirectional graphite fibers crosslaid with 1 ply of No. 112 fiberglass cloth between graphite composite plies using Narmco No. 5505 Epoxy impregnation; total thickness approximately 0.009 in.
° Core	1/4" x 5052 x .007P-16 x 0.375" thick aluminum honeycomb; approximately 1.6 lb./ft^3.
° Adhesive	Narmco No. 252; approximately 0.0015 thick.
Cellstack	
° Coverglass	Dow Corning 0211 microsheet; 0.006 in. thick.
° Coverglass Adhesive	Dow Corning R6-3489.
° Silicon Cell	2 cm. x 4 cm. x 0.014 inches thick.
° Cell-to-Substrate Adhesive	G.E. RTV-118
° Dielectric	0.001 in. thick Kapton.
° Interconnects	0.0015 in. Kovar.
° String Collector Bars	0.003 in. Kovar.
Module	
° Overall Dimensions	30" x 48" x 0.400" thick.
° Total Weight (Including Test Support Inserts and Hinges)	6.43 lbs.
° Specific Weight	0.643 lb./ft.^{2}
° Packing Factor	0.93
° Specific Power (AMO, 28° C, 1AU)	12 watts/ft.^{2} 17.5 watts/lb.

3. CONCLUSIONS AND RECOMMENDATIONS

3.1 CONCLUSIONS

This phase of the lunar surface power system development program has resulted in confirming the flight readiness of the Prototype Module. This has been demonstrated by the successful completion of the qualification test program as outlined in the Reference 1.5 Test Plan, and as documented in Section 6 of this report.

The emphasis in this program has varied throughout the various phases. During Phase I, the prime objective was to develop parametric data for the use of large area solar arrays on the lunar surface. This data was documented in Reference 1.1. The new technology associated with this phase consisted of the conceptual design of three array configurations, namely, flat, oriented-skirted and lean-to. For the proposed lunar surface mission, a $45KW_e$ lean-to array was selected as the candidate configuration. During Phase II, the objective was to transpose this candidate configuration into hardware. A baseline 30 in. x 48 in. Engineering Test Module (ETM) was established and three configurations employing different substrate technology were designed, fabricated, and development tested. The three configurations were designated ETM I (fiberglass lattice on pre-stressed aluminum box beam frame), ETM II (two flexible Kapton modules contained between aluminum honeycomb end modules), and ETM III (graphite composite facesheets on lightweight aluminum honeycomb core). The details of these designs, as well as the test results, were documented in Reference 1.2. This program phase served to develop new technology associated with light-weight solar array modules in the 12 to 18 watts/lbs. range, capable of surviving the temperature extremes (-173°C to +120°C) of lunar surface operation. In addition, it uncovered a new cellstack failure mode designated silicon cell spalling.

Phase III was initiated to establish the critical design parameters associated with this spalling phenomenon. These were identified as adhesive thickness, coefficient of expansion, and modulus of elasticity. The variations in the coefficients of expansion of the various materials used in the cellstack/substrate components were the prime stress-producing

factors. However, the occurrence of spalling was found to be directly related to the stress level reached in the adhesive/silicon cell bond region. This program phase succeeded in identifying the critical parameters associated with spalling utilizing both analytical and experimental techniques and was documented in Reference 1.3.

The new technology results of these earlier phases were incorporated into the design of the Prototype Module in Phase IV. The successful passing of the qualification tests imposed on this module confirmed the adequacy of the new techniques utilized in the design of the overall cellstack/substrate configuration. The design techniques associated with this Prototype Module are considered to be technology-ready for future lunar surface, planetary, and earth-orbital applications.

3.2 RECOMMENDATIONS

This lunar surface power system program has resulted in the development of new technology associated with solar array substrate and cellstack design. However, the ultimate performance and sizing of solar array modules is a function of various time-independent and time-dependent degradation factors. As power levels increase to $25KW_e$ and beyond, and a 10-year operating life becomes a design goal, it would appear important to reassess the various performance degradation factors normally utilized by industry in solar array design. It is recommended that several of these degradation modes be investigated both analytically and experimentally, with a view towards establishing more realistic and improved design margins. The following degradation factors are recommended for further assessment and evaluation.

3.2.1 The use of coverslides or coatings to protect the silicon cell from ultra-violet radiation degradation results in a decrease in the transmissible solar intensity. Nominally equal to 139.6 mw/cm^2 (1 AU, AMO), a loss of 4.0 to 9.0%in ten years is estimated. To insure protection against UV radiation, a cutoff wavelength of 0.41 um is desired. Fused silica or Dow Corning 0211 microsheet are commonly used coverslide materials. A high transmissibility adhesive such as Dow Corning R6-3489 is employed to bond the coverslide to the silicon cell. Spray-on materials or integral coverslides are also considered. It is proposed to analyze these various

approaches, as well as exploring new techniques to reduce this degradation factor. A test program utilizing a coverslide matrix test model similar to the Phase III cellstack bonding matrix (Figure 8.1 of Reference 1.3) would also be employed.

3.2.2 Radiation Degradation Due to High Energy Electrons causes a considerable loss in end-of-life (EOL) power. For long duration missions fluence levels as high as 1×10^{14} to 1×10^{16} electrons/cm^2/year can be experienced. Depending on cellstack design parameters such as cell thickness, base resistivity, cell dimensions, and coverslide thickness, it is possible to experience a power loss for a 10-yr. life as high as 50%. However, the estimation of the exact magnitude of this loss can vary with the assumptions made in establishing the radiation degradation model. This model is a function of laboratory test data, satellite and spacecraft flight data, and various trapped particle data. This radiation degradation is also a function of orbital altitude and inclination and solar flares. Because of the complexity of this degradation mode, various differing criteria exist in both industry and government agencies for its determination. With the advent of very large solar arrays, the disparity that exists between these various sources becomes significant in establishing adequate design margins. It is proposed to assemble and analyze the existing radiation degradation data and to quantify it into a standard model for use by both government and industry. In addition, in those areas where sufficient data is lacking, it is recommended that laboratory tests be conducted over a wide range of silicon cell types and geometries to provide an adequate statistical base for evaluation of this degradation mode.

3.2.3 Temperature Cycling can have a major impact on solar array power degradation. The most common failure mode experienced due to this environment is solder joint or interconnector fatigue. This results in open connections, which despite the use of redundancy leads to decreased power output. Additional performance degradation can result from the temperature extremes associated with this phenomenon. Thus, high temperatures decrease the cell output voltage due to increased series resistance and cause solder melting or creep; and extremely low temperatures can give

rise to silicon cell spalling and adhesive bond failures. Insufficient parametric and test data exists to adequately assess these various degradation modes so that proper design margins can be applied. It is proposed to establish an analytical model which would include all the design parameters that are involved in this degradation mode. This would include substrate and cellstack material properties, geometrics, heat transfer characteristics, electrical criteria, and stress considerations. Because of the complexity of this pheonomenon, a computer program would be generated to permit assessment of all the variables and the impact of potential interactions. The sensitivity of the various design parameters to array power degradation would also be determined. It is further recommended that a comprehensive test program be established and implemented to confirm the validity of the analytical results.

3.2.4 Radiation Degradation Due to Low Energy Protons can cause very high power losses at higher orbital altitudes. Proper shielding of the silicon cell with coverslides can reduce this degradation mode. However, a comprehensive analytical model to establish adequate design margins in this area is still lacking. It is recommended that this degradation mode be analyzed in sufficient depth so that proper design margins can be established which do not result in excessive weight penalties to achieve required shielding goals.

3.2.5 Micro-Meteorite Degradation for earth orbital applications has usually been assumed not to exceed 1 to 2%. However, as solar array areas and mission durations increase, this degradation factor will become more pronounced. Probability of experiencing micro-meteorite damage is a function of both array frontal area and exposure time. The magnitude of this damage relates to particle size and velocity. Various environmental models exist for estimating the micro-meteoroid flux and secondary ejecta flux. However, here again sufficient disparity exists to make it difficult to arrive at optimum design margins. It is proposed to examine the various environmental criteria and establish an analytical model that best represents this degradation mode. A probabilistic approach is envisioned since this degradation mode must be based upon statistical factors. It is further recommended that this analytical model form one

of the criteria for preparation of standard solar array performance specifications.

3.2.6 As solar array power outputs and voltage levels increase, it becomes necessary to reassess the prevailing design criteria for achieving electromagnetic compatibility. This factor, while not directly related to array performance degradation, can directly influence solar array circuitry and power transmission cabling design. This, in turn, can result in weight penalties to provide acceptable electromagnetic interference levels. It can also impose the necessity of incorporating additional shielding and circuitry in sensitive experiment packages. It is proposed to analyze the various electromagnetic characteristics of solar arrays operating over a range of voltages and utilizing various cell string arrangements. This analysis should also include the use of shunt and blocking diodes and the potential creation of electromagnetic interference fields resulting from random shorting or open circuits. Finally, it is recommended that this analysis include an assessment of twisted-wire cabling and flat cabling, and any other magnetic field-producing materials that might potentially be used as candidate components for large, high-powered solar arrays.

4. PROTOTYPE MODULE DESIGN

4.1 SUBSTRATE DESIGN

The Prototype Module substrate design was the same as that employed on Engineering Test Module III. This design is shown on TRW Systems Drawing No. SK 120044-Rev. 1 (Figure 2.1). The substrate consisted of a 0.375 inch thick aluminum honeycomb core (1/4 x 5052 x 0.0007P-16). This core has a density of 1.6 lbs./ft^3. When used together with Morganite Type II graphite composite facesheets, it results in the lightest rigid substrate that has been built in this size. This 30" x 48" substrate was the design used for the Prototype Module. Inserts were provided on the module sides for mounting to the test fixture during structural-dynamic testing.

4.2 CELLSTACK DESIGN

A decision was made during this program phase to use 2 cm x 4 cm silicon cells. The use of RTV-118 cell-to-substrate adhesive was planned based upon the test results of Phase III. An analysis and layout was made to determine a suitable series/parallel arrangement for the 2 cm x 4 cm silicon cells. A submodule consisting of two cells in parallel and 33 cells in series appeared attractive. By employing two of these submodules in a string consisting of two cells in parallel and 66 in series, an interconnected cell area of approximately 178 sq. in. results. This configuration permitted seven of these interconnected strings to be installed on the module substrate (see Figures 2.1 and 2.2). The approximate power output from each of these strings is 16 watts at 31 volts (at AM0, 28°C, and 1 AU). This is equivalent to 12.0 watts/ft^2. This cell arrangement resulted in a total of 924 interconnected cells with a total power output of 112 watts. The specific power for the overall module is 17.5 watts/lb. for a Prototype Module weight of 6.43 lbs.

An additional analytical assessment of the silicon cell/RTV adhesive, thermal vacuum-induced stresses was conducted during this phase. The results are given in Appendix A. This data indicated that if scratches or micro-cracks at the silicon cell/RTV adhesive interface were present, spalling of the silicon cells could take place at stress levels

considerably below the values of the silicon cell ultimate tensile strength. This latter value is nominally 19,000 psi for random crystal orientation cells (Centralab type) and approximately 28,000 psi for the preferred crystal orientation cells (Heliotek type).

A meeting was held at Centralab, El Monte, California, on 2 March 1971 to review the results of Phase III of this program. The influence of the surface finish on the back side of the silicon cell and its possible impact on spalling was discussed. It was revealed that the mechanical shaping operations, such as sawing, lapping, and mechanical and/or chemical polishing can introduce work damage into a semiconductor such as silicon (see Reference 1.6). In view of this, approximately 200 cells, representing seven different types, were obtained from various sources. These were used to conduct a low temperature (-173°C) thermal test to check the adequacy of the adhesive bond. The types of cells utilized and their location on the test module is shown in Table 4.1. All the cells were 0.012 to 0.014 inches thick and bonded to an aluminum facesheet substrate using either RTV 3145 or RTV 118. All the adhesive thicknesses were maintained at a nominal 0.005 inches. The test module, with the arrangement and location of cells used, is shown in Figure 4.1. This test module was subjected to low temperature thermal cycling. The module was cycled in steps from room temperature (23°C) to three lower level temperatures, i.e., -135°C, -150°C, and -173°C. This procedure was followed to determine if spalling would occur at some minimum temperature above -173°C. Two low-temperature soak cycles at -173°C were conducted (four hours and eight hours respectively).

At the completion of this test, it was found that all the silicon cells had successfully passed. No spalling occurred regardless of which adhesive was employed or what type of cell was involved. This test indicated that adhesive thickness, rather than cell bondline surface finish, is the more significant parameter with respect to the inception of spalling. As a result of this test, a decision was made to use 2 cm x 4 cm silicon cells similar to the type being used for the Skylab I solar arrays.

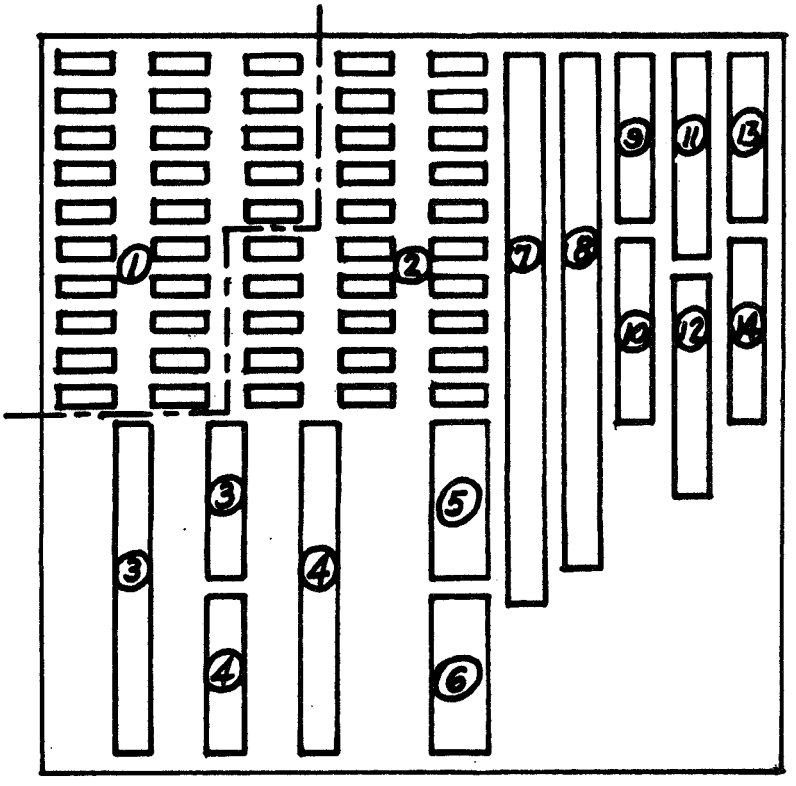
During these thermal cycling tests, four 2 cm x 4 cm silicon cells

were interconnected with 0.0015 inch Kovar interconnects similar to that shown on Figure 2.2. These were bonded to an aluminum plate and subjected to one thermal cycle test down to -173°C. The interconnects and solder joints were inspected at the completion of this test and found to be unaffected. The parallel interconnects and the negative and positive bus bars were analyzed and found to be adequate to meet the structural-dynamic and thermal environments.

TABLE 4.1 - TYPE OF SILICON CELLS USED FOR THERMAL CYCLING TEST

AREA	1	2 x 4 Preferred Crystal Orient - RTV 3145
"	2	2 x 4 Preferred Crystal Orient - RTV 118
"	3	2 x 2 Chem Polish Pref Crystal Orient Solder Dipped - RTV 3145
"	4	2 x 2 Chem Polish Pref Crystal Orient Solder Dipped - RTV 118
"	5	2 x 4 SAS Cells - RTV 3145
"	6	2 x 4 SAS Cells - RTV 118
"	7	2 x 2 Chem Polish Pref Crystal Orient No Solder - RTV 3145
"	8	2 x 2 Chem Polish Pref Crystal Orient No Solder - RTV 118
"	9	2 x 2 Mech Polish Alum Contact - RTV 3145
"	10	2 x 2 Mech Polish Alum Contact - RTV 118
"	11	2 x 2 M35 Zone Solder - RTV 3145
"	12	2 x 2 M35 Zone Solder - RTV 118
"	13	2 x 2 M35 Solder Dipped - RTV 3145
AREA	14	2 x 2 M35 Solder Dipped - RTV 118

ALL BOND LINES SHIMMED TO 5 MILS



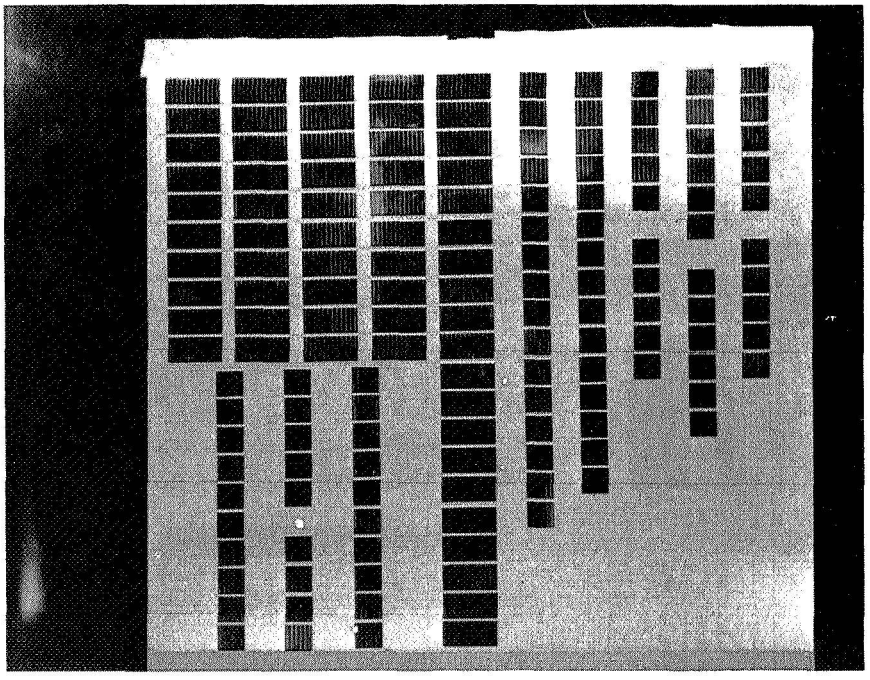


Figure 4.1 Cell Adhesive Bond Test Model

5. PROTOTYPE MODULE FABRICATION

5.1 MANUFACTURING CONSIDERATIONS

The fabrication of the Prototype Module was implemented in a manner similar to that of the ETM III which was built during Phase III of this program. One small modification was that this time the drawing-specified light-weight (1.6 lb/ft^3) honeycomb core was employed, rather than the heavier (3.0 lb/ft^3) one previously used.

Upon completion of the manufacture of the substrate, in accordance with Figure 2.1, it was noticed that a slight bow had occurred of approximately 0.25 inch in 48 inches. This was acceptable for use in this program. However, the phenomenon was investigated and it was determined that with the new, light-weight core utilized, it was important to achieve a so-called balanced substrate structure. This meant assuring that the graphite filaments in the outer plys of the facesheets ran in the same direction. The drawing was revised to incorporate this requirement and no further difficulty in this area is anticipated.

The cellstack was fabricated utilizing manufacturing techniques similar to that employed on the Skylab I solar array. However, since a flat laydown design rather than an overlap design was desired, new submodule fixturing was required. Submodule elements consisted of two cells in parallel by 11 cells in series. These were mounted on the substrate and interconnected to produce seven strings of two cells in parallel by 66 cells in series. A total of 924, 2 cm x 4 cm silicon cells were mounted on the module substrate using RTV 118 adhesive. To stay within the scope of this program phase, the cells utilized were mechanically sound but exhibited electrical performance slightly too low to be acceptable for use on the Skylab I solar array.

The completed panel was inspected and a record made of any non-critical cosmetic defects. All seven strings were electrically tested on the TRW Systems Xenon Flash Tester (P/N X 311693 - S/N 001). The results of these I/V performance tests are shown in Appendix B. The panel was tested at room temperature (25°C). Electrical performance was checked against a calibrated standard cell (TRW No. SAS-CL-173;(261.1 mA)).

The insulation (Kapton) resistance and isolation between individual strings were checked for shorts and none were found.

The completed Phase IV Prototype Solar Array Module is shown in Figure 5.1. This module is 30 in. x 48 in. by approximately 0.400 in. thick. The module includes four hinges and weighs 6.43 lbs. This results in a specific weight of 0.643 lb./sq. ft. The 924 cells mounted on it results in a packing factor of 0.93. At a nominal performance of 12 watts/ft^2 for AMO, 1 AU, 28°C conditions, this module has a specific power of 17.5 watts/lb.

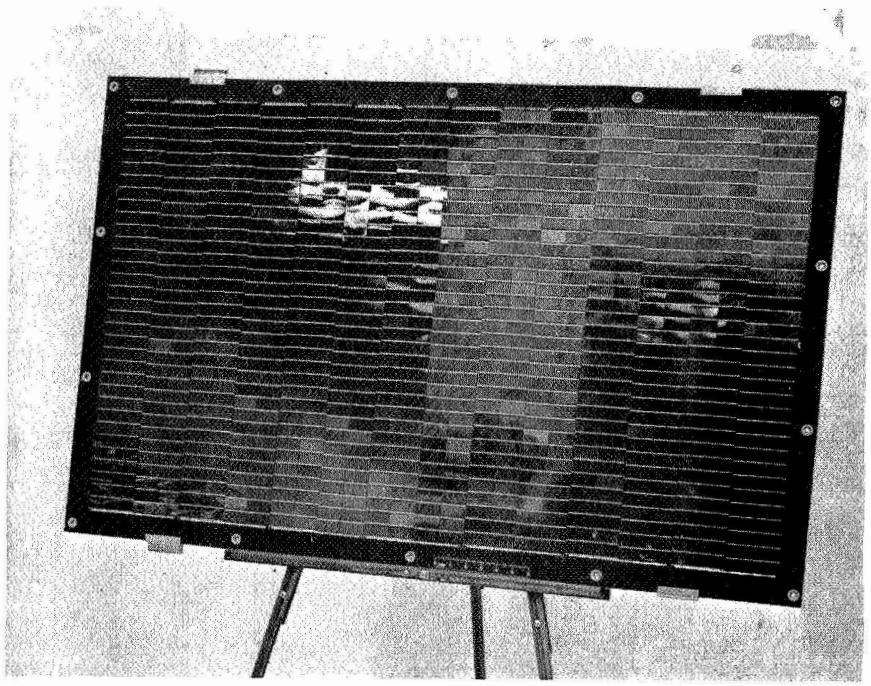


Figure 5.1 Phase IV Prototype Solar Array Module

6. PROTOTYPE MODULE TEST EVALUATION

6.1 TEST OBJECTIVES

The primary purpose of this test program during this phase of the development effort was to qualify the Prototype Test Module. The Qualification Test requirements are described in Reference 1.5. They consist primarily of 3-axis random and sinusoidal vibration, thermal vacuum cycling, and acoustic tests. An additional objective of this test program was to confirm the validity of the adhesive bonding development results of Phase III and the adequacy of the flat laydown interconnect design. Finally, electrical performance characteristics (I/V curves) were to be obtained for all the cell strings at the beginning and upon completion of these qualification tests.

6.2 TEST OPERATIONS

The Prototype Module was shipped to NASA/MSFC. TRW Systems visited NASA/MSFC on May 6, and 7, 1971, to witness receipt of the module and the structural-dynamic portions of the qualification tests. Visual inspection upon its arrival indicated that it was in good condition. It was then transferred to the NASA/MSFC Astrionics Laboratory Environmental Test Area. Visual inspection at this point indicated that the interconnects supporting two of the Kovar collector strips had accidentally been bent through 90° by a technician when unpacking the module in the test area. These were left in this position, since bending them back to their normal flat position might excessively work-harden the supporting interconnects. The module was mounted on the shake table. At this point, due to lack of communication, another technician bent the previous two Kovar collector strip interconnects back to their flat position. This was not desirable, but the testing was initiated.

6.2.1 Structural-Dynamic Testing

Sinusoidal, random high-level and random low-level vibration tests were performed on the Prototype Module. The vibration survey was conducted in each of three mutually perpendicular axes using the levels specified in Reference 1.5. (See Figure 6.1 for test setup.)

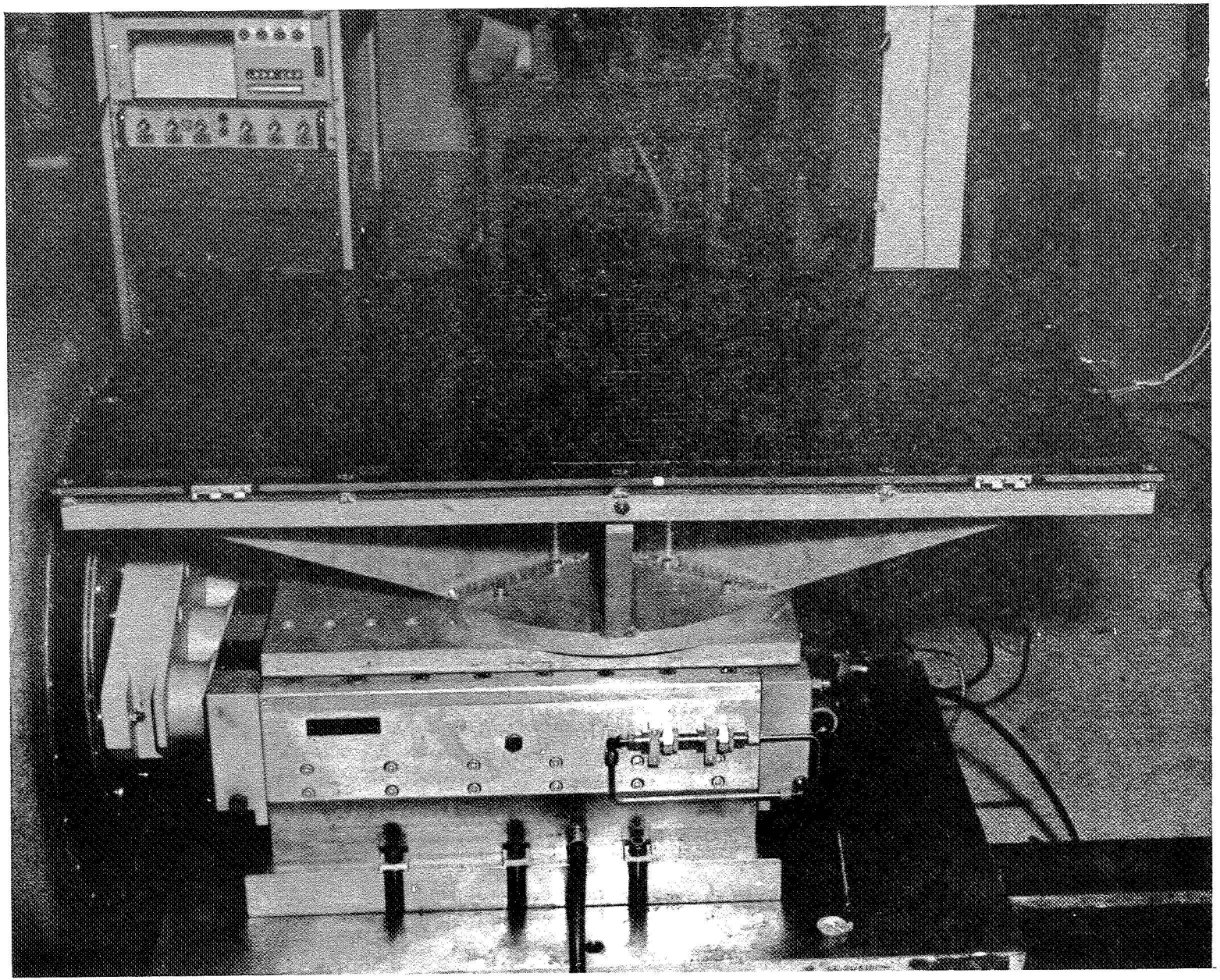


Figure 6.1 Test Setup of Prototype Module for Structural-Dynamic Testing

During the"X"axis test (excitation in a direction parallel to the cellstack surface), several of the string collector strips broke loose. It was originally planned to bond these to the substrate with adhesive. However, a decision was made to omit this step during manufacturing. It was felt at that time that the four to eight interconnects supporting these collector strips would be strong enough to support these collector strips. By omitting this operation, costs on future production modules could be reduced. However, as the testing proceeded, additional collector strip-supporting interconnects continued to break and it became obvious that the collector strips should have been bonded down to the substrate. To permit the testing to proceed, as breaks occurred the partially broken end interconnects were taped to the substrate to preclude the possibility of cell damage.

During the "X" axis sinusoidal test (excitation parallel to the cell surfaces and along the 48-inch dimension of the panel), the shake table control accelerometer broke off the test fixture. The malfunction caused the Prototype Module to be subjected to vibration levels higher than specified test conditions. These overload levels were later experimentally determined by using a dummy panel and duplicating conditions during the malfunction run. It was found that the worst case over-test levels occurred at approximately 975 Hz and varied from 500g rms to 800g rms measured in the "X" axis direction. A 5g to 7g rms input was required to the slip table in the "X" axis direction in order to duplicate the malfunction conditions. This represents a g-load input of from 2 to 2.8 times the test-specified input of 2.5 g's.

It was decided to continue with the qualification testing despite the fact that the panel had been overloaded during the shake table malfunction. It was recognized that this severe overload condition could be reflected in producing interconnector failures that would not have occurred under normal specified load conditions. However, by inspecting and documenting the failures that had occurred at the completion of the structural-dynamic tests, it was then possible to evaluate the test results upon completion of the acoustic and thermal vacuum tests.

The structural-dynamic tests were completed. An examination of the

panel at the end of these tests revealed that the cellstack (exclusive of interconnects) had successfully passed these tests. It was further determined that out of a total of 3,696 interconnector tabs, only 28 interconnect tabs were found broken after all testing had been completed. This constitutes less than 0.8%. Furthermore, all of these occurred on the interconnect tabs on the outer row of the silicon cell strings and may have been a result of the overload test condition. Some of the broken interconnects (8) were found after post-test electrical data indicated a noticeable drop in one of the module strings short circuit current reading as compared to the pre-test data. The other broken interconnects were found by visual inspection in strings that had no degradation in short circuit current (Figure 6.2). This confirmed the inherent reliability of the redundancy resulting in using four interconnect tabs per cell. It was concluded from these tests that the basic interconnect design was satisfactory. However, to confirm the adequacy of the collector strip design, a test sample (Figure 6.3) was fabricated at TRW Systems. The collector strip was identical to that used during structural-dynamic testing at NASA/MSFC, except that in this case it was bonded to an aluminum plate substrate. Two bonding configurations were utilized. In one case, the collector strip was bonded using two Silastic 140 adhesive dots. Four adhesive dots were employed on the other collector strip. This sample was mounted to a Ling, 15,000 lb-force shake table, as shown in Figure 6.4. The test sample was then subjected to both sinusoidal and random vibration testing in the "X" axis. Both bonding configurations were found to be completely satisfactory. There was no evidence of damage, either to the collector strips or the supporting interconnects. It was mutually agreed that upon successful completion of the remaining qualification tests the Prototype Module would be shipped back to TRW Systems so that new collector strips and associated interconnects could be installed and bonded to the substrate. This was done and the "X" axis testing was repeated at NASA/MSFC. These tests were completely successful, thus confirming the ability of the Prototype Module to meet the structural-dynamic requirements of this program.

6.2.2 Acoustic Testing

The acoustic tests were performed in accordance with Reference 1.5.

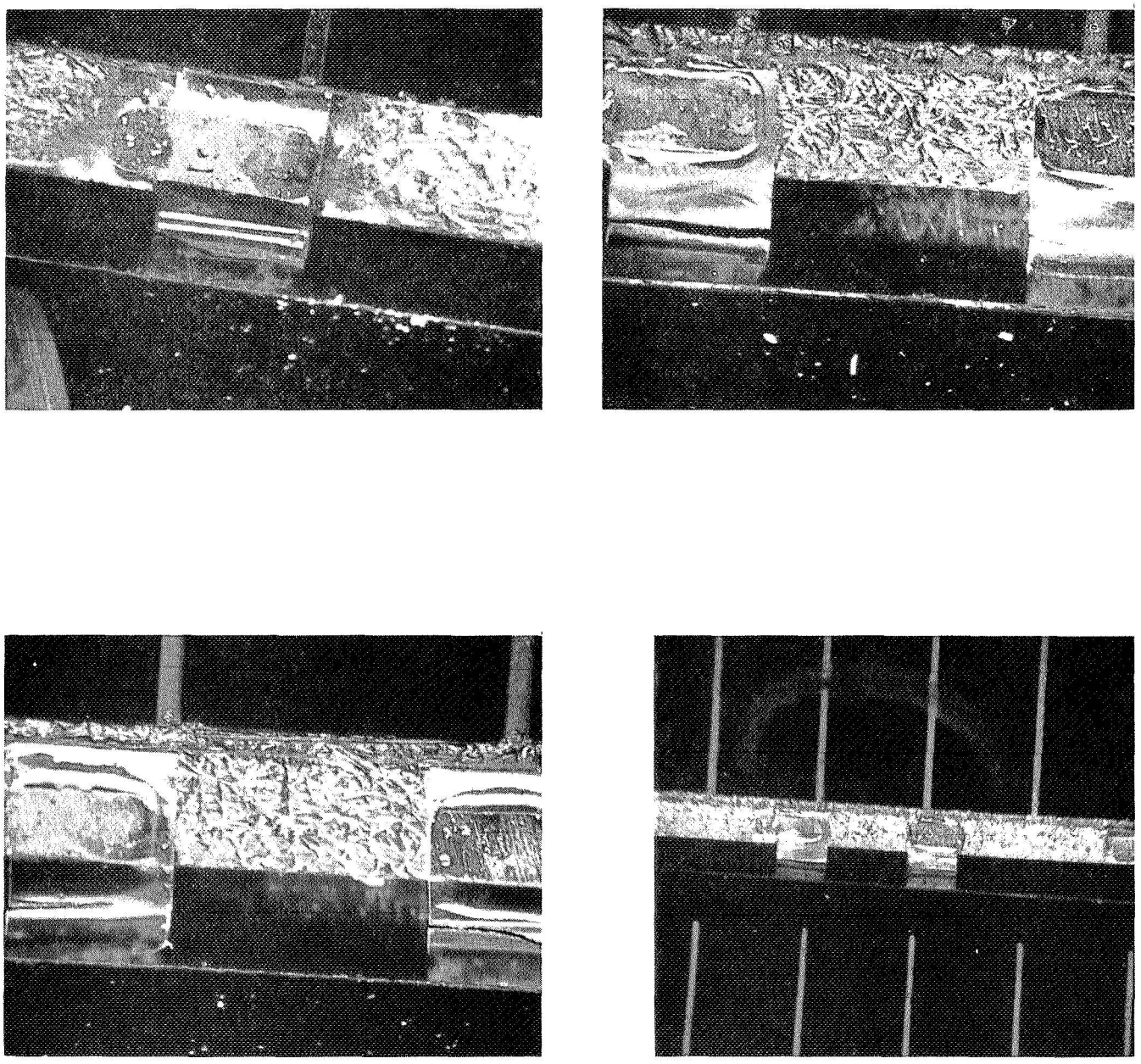


Figure 6.2 Typical Interconnector Failures
During Structural-Dynamic Testing

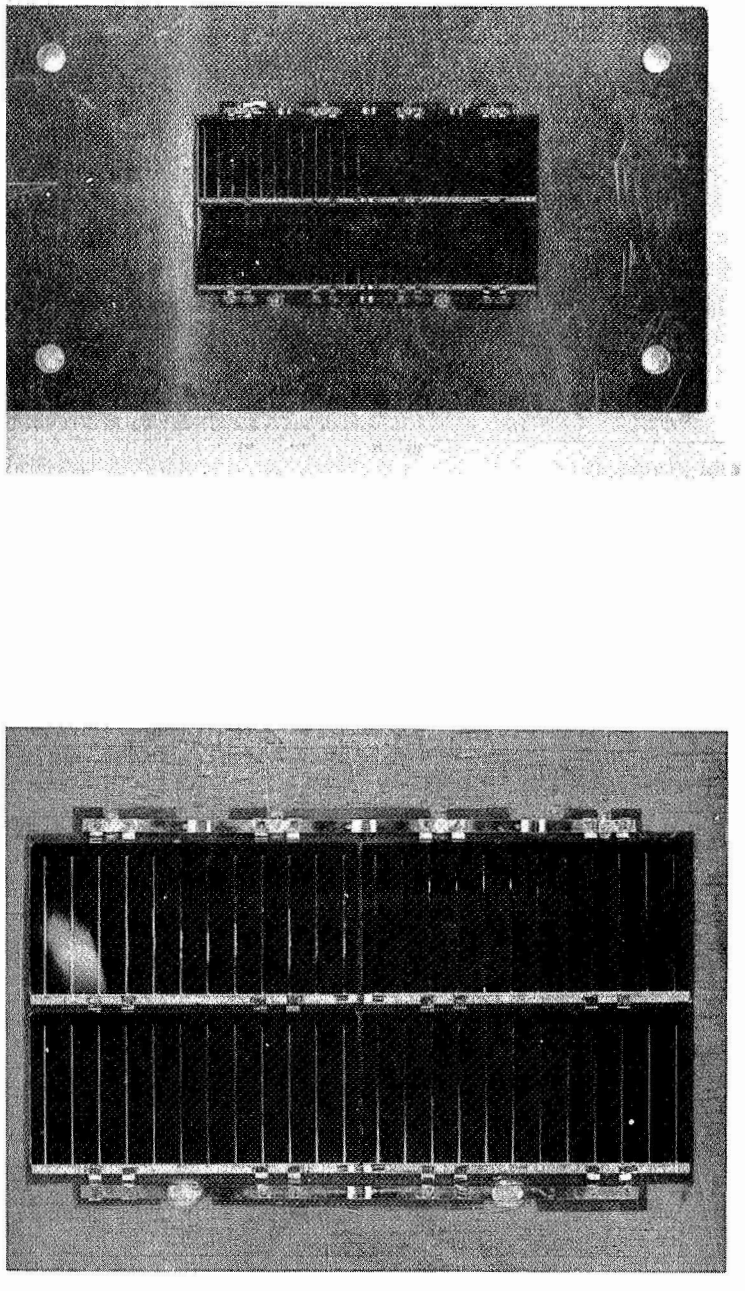


Figure 6.3 Collector Strip Test Sample

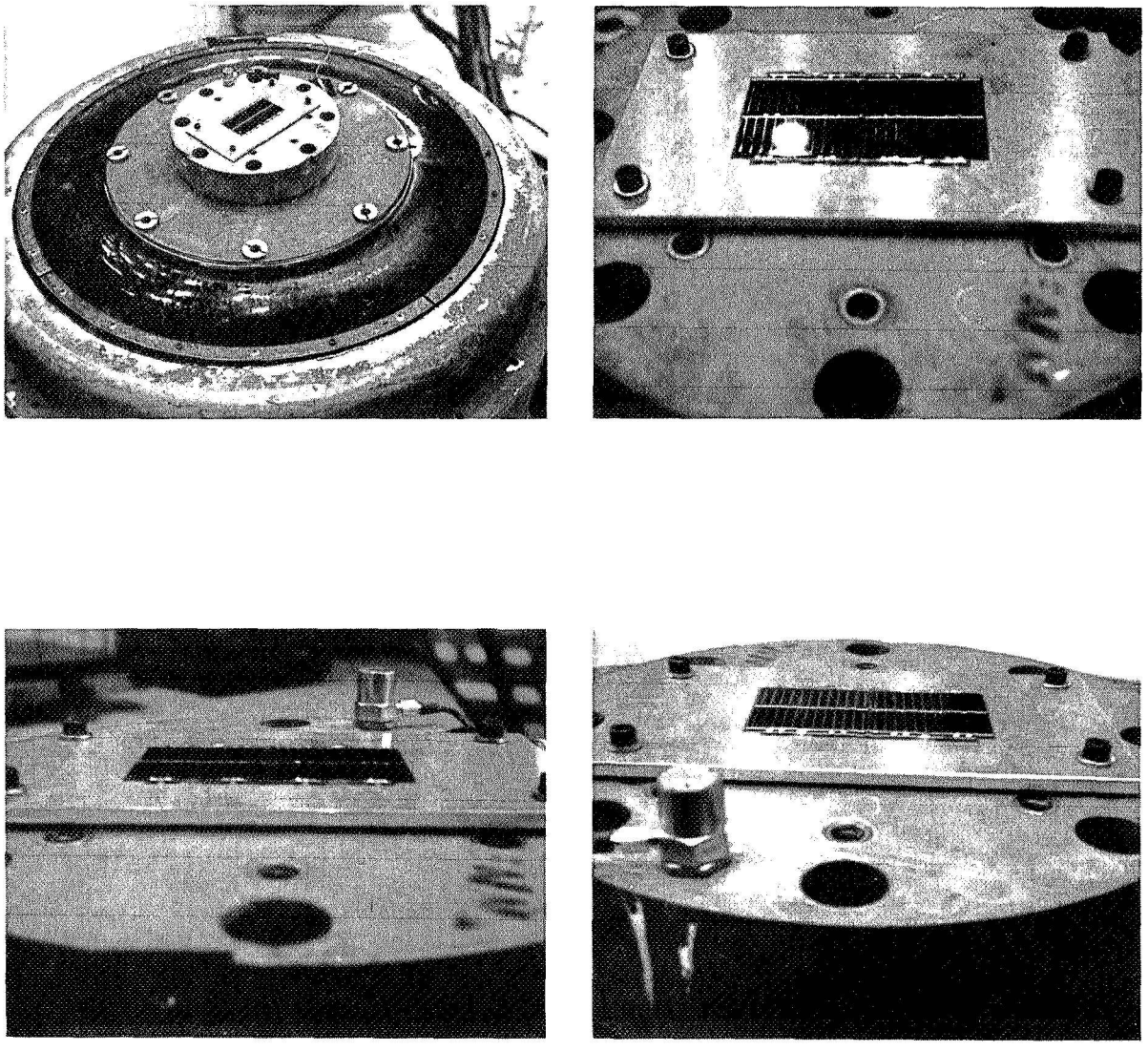


Figure 6.4 Collector Strip Test Sample - Test Setup

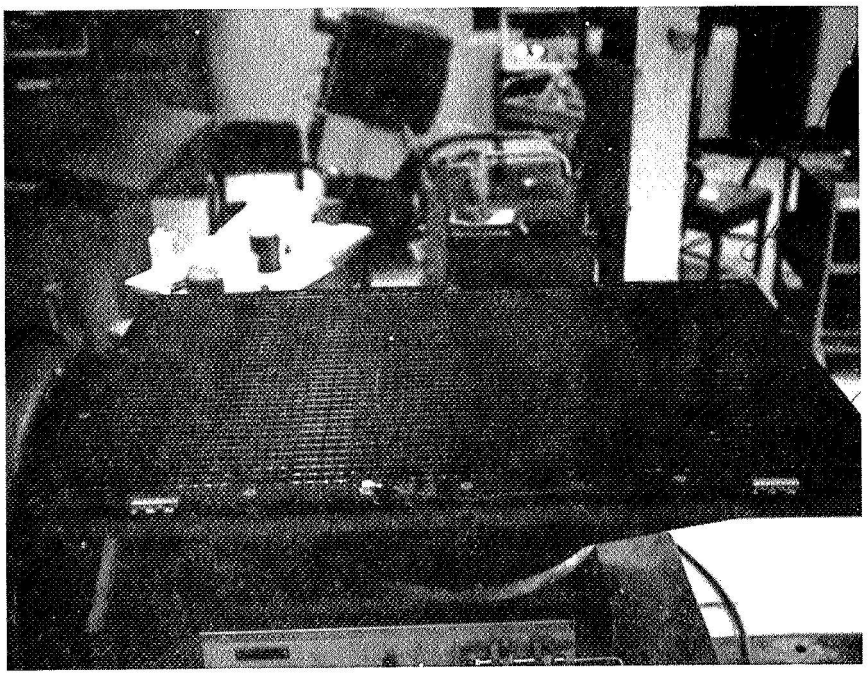
The test setup was similar to that utilized during Phase II (see Figure 8.28 of Reference 2). The test on the Prototype Module was initiated after the test setup had been checked out using a dummy panel in the reverberation chamber. No damage was experienced during these tests despite subjecting the module to acoustic energy levels as high as 156 db. It was concluded that the Prototype Module had successfully passed these tests.

6.2.3 Thermal Vacuum Testing

The thermal vacuum testing was conducted in accordance with Reference 1.5. This consisted of subjecting the Prototype Module to two 12-hour cycles over a temperature range from +120°C to -173°C. Sufficient time was allowed at both the peak and low temperature regimes to assure stabilization of the module temperature. The Prototype Module successfully passed these tests and confirmed the adequacy of the adhesive bond design. It provided additional verification of the analytical and experimental results conducted in Phase III which resulted in establishing the criteria for the elimination of the spalling phenomenon which had occurred during Phase II of this program.

6.2.4 Test Evaluation Summary

The Prototype Module was subjected to all the environments it would normally experience during a lunar surface mission. This includes Saturn V launch, trans-lunar, lunar landing, and lunar surface operation modes. It is concluded that with the incorporation of the bonded collector strip design modification, the Prototype Module successfully passed its required qualification tests and can now be considered a flight-ready design for future lunar surface solar array applications. The qualified Prototype Module is shown in Figure 6.5 at the completion of all tests.



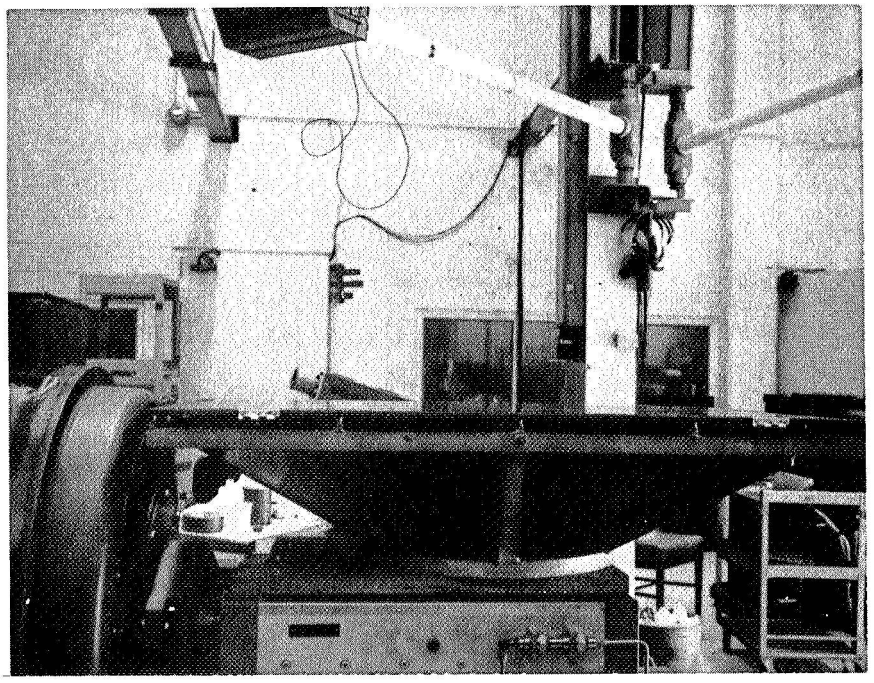


Figure 6.5 Prototype Test Module at Completion of Qualification Testing

REFERENCES

1.1 "Study to Establish Criteria for a Solar Cell Array for Use as a Primary Power Source for a Lunar-Based Water Electrolysis Systems - Phase I Final Technical Report"; TRW Systems Report 09681-6002-R000 of 30 June 1968.

1.2 "Study to Establish Criteria for a Solar Cell Array for Use as a Primary Power Source for a Lunar-Based Water Electrolysis System - Phase II Final Technical Report"; TRW Systems Report 09681-6005-R000 of 15 November 1969.

1.3 "Study to Establish Criteria for a Solar Cell Array for Use as a Primary Power Source for a Lunar-Based Water Electrolysis System - Phase III Final Technical Report"; TRW Systems Report 09681-6007-R000 of 15 December 1970.

1.4 TRW Systems Proposal 09681.005, "Study to Establish Criteria for a Solar Array for Use as a Primary Power Source for a Lunar-Based Water Electrolysis System - Volumes I and II", of 5 August 1970.

1.5 "Test Plan - Engineering Test Model of LEPEPS Solar Array"; TRW Systems Report 09681-6004-R000 of 4 December 1968.

1.6 "Depth of Work Damage Resulting from Shaping Operations on Silicon"; Whitten, W. N.; Heitz, A. J.; and McNamara, J. E.; 126th Meeting of Electrochemical Society, Washington, D. C., 13 October 1964.

APPENDIX A

ADDITIONAL ASSESSMENTS OF SILICON CELL/RTV ADHESIVE THERMAL VACUUM-INDUCED STRESSES

1.0 INTRODUCTION

At the completion of the Phase III effort on this program, it was determined that the allowable silicon cell ultimate tensile stress in the upper layers of the silicon (i.e. 0.00001 to 0.00017 inches below the silicon/RTV interface) was a critical factor in determining if spalling would occur. It was concluded that either surface scratches or microcracks induced by bending of the silicon cells during the manufacturing operation could considerably lower the actual allowable ultimate tensile stress of the silicon. This, in turn, could have an impact on the allowable material properties of the RTV adhesives at low temperature. During Phase IV, it was important to select the proper design criteria for both the silicon cells and the RTV adhesive to insure successful passing by the Prototype Module of the thermal-vacuum qualification testing. Because of this, a refined analysis was conducted during the early portion of Phase IV, to enhance the judgement factor in arriving at the design requirements for the prototype module cellstack.

2.0 BASIS FOR ANALYSIS REFINEMENT

Spalling of silicon solar cells starting at the edges of the RTV bond dot is a serious problem encountered during thermal cycling to -173°C. The silicon thermal stresses had been previously analyzed using a finite element structural analysis program, and were parametrically studied with RTV bond parameters varying, as presented in the Phase III- Final Technical Report (TRW Report No. 09681-6007-R000 of 15 December 1970). Silicon stress, f, at a plane 0.00017 inch below the silicon/RTV interface was shown to follow a simple formula:

$$f = (N_o)[a + b/N_o] \quad ; \quad a = 280.754$$

$$N_o = \alpha_2 t_2 E_2 \, (-\Delta T) \qquad b = 1347.842 \quad \text{(Curvefit)}$$

where:

N_o = "Bimetallic strip" interface load

α_2 = RTV thermal expansion coefficient, assumed constant at given temperature, T

E_2 = RTV elastic modulus, assumed constant at given temperature, T

t_2 = RTV thickness

$(-\Delta T)$ = Temperature decrease (+)

The primary difficulties are the variation of E_2 and α_2 RTV adhesive mechanical properties with temperature and the uncertainty of allowable silicon stresses, f, at an arbitrary sub-surface plane.

3.0 APPROACH TO ANALYSIS REFINEMENT

In order to account for material property temperature variations of the RTV adhesive, a refined definition of material parameters, S, is utilized:

$$S = E_T \int_{T_o}^{T} \alpha \, dt \quad [psi]$$

where E_T is the Young's elastic modulus at the low temperature, T, and α is the varying thermal expansion coefficient over the temperature range from T_o, room temperature, down to T, the minimum low temperature assumed. The integrated expansion coefficient has the physical meaning of an overall unloaded thermal strain of the RTV adhesive as the temperature is decreased. The parameter, S, therefore represents axial stress in the RTV adhesive bond.

Silicon thermal stress, f_s, at 0.00017 inch below the silicon/RTV interface surface, is defined by the following equation:

$$f_s = [aSt + b]$$

t = RTV bond thickness
a and b same constants as found in Phase III study

where St replaces N_o and is set by the value of f_s

A plot of the allowable RTV adhesive material property parameter, S, versus RTV thickness, t, and maximum sub-surface silicon stress, f_s, is presented in Figure A-1. The equation for silicon stress, f_s, is completely defined by the value of the material property, Rt. This is equivalent to S varying by C/t where the constant, C, is defined by the following equation:

$$C = [f - b]/a$$

These curves, for four values of silicon sub-surface stress, f_s, are plotted in Figure A-1.

4.0 IMPACT ON PHASE III RTV ADHESIVE TEST DATA

Four types of RTV adhesive bond materials were tested to obtain thermal expansion coefficient and elastic modulus versus temperature, and were also

utilized in cellstack thermal cycle tests. Predicted interface surface silicon thermal stress varied from 1380 psi for the PR-1538 adhesive to 5384 psi for the RTV-118 adhesive. The lowest predicted stress of 1380 psi, with PR-1538, was never verified because of inadequate bond adhesion, which caused bond failures and masked any tendency to detect silicon spalling. The next lowest predicted stress of 2155 psi, with RTV-3145, however, resulted in a high incidence of silicon spalling, due to assumed pre-stresses in the larger 2 x 4 cm cells used with this adhesive. The cells are flattened from their pre-curved as manufactured state, inducing pre-thermal bending stresses. The RTV 511/577 adhesive resulted in a predicted stress of 2855 psi, and no failures were noted. The RTV-118 adhesive resulted in a predicted stress of 5343 psi and a correspondingly higher incidence of silicon cell spalling was noted during thermal testing.

The conclusion from this analysis is that spalling can be prevented in non-prestressed silicon solar cells if the sub-surface thermal stress (with microscopic stress concentration factors not included) can be held below about 3000 psi at -173°C. This can be done if the product St can be maintained below a value of 5.88 lb/in.

5.0 EFFECTS REDUCING APPARENT SILICON STRENGTH

The sub-surface allowable silicon stress of 3000 psi, as determined in thermal testing, is well below the apparent strength of 19000 psi. The following mechanisms account for the apparent discrepancy:

5.1 Surface to Sub-surface Stress Ratio: The calculated stress at an arbitrary level 0.00017 inch below the RTV/silicon interface surface is well below the actual maximum stress at the surface. Based on the stress distribution determined in earlier finite element analysis, a factor of about four should be used to ratio stress at the two locations within the silicon cross-section.

5.2 Microscopic Stress Concentrations: Because of the relatively low ductility of silicon, any surface scratches or pits will cause significantly higher local stresses to occur in their vicinity and initiate spalling failures.

5.3 Pre-stress Due to Cell Bowing: In the case of relatively large silicon cells, the manufacturing process sometimes

introduces cell curvature. Bending pre-stresses are subsequently setup across the cell upon straightening, and these pre-stresses are then added to thermal differential expansion stresses under thermal cycling.

5.4 Silicon Strength Variation: Based on representative structural tests on silicon blanks, the material strength has been shown to vary considerably from vendor to vendor and even from batch to batch. The design strength of 19,000 psi may not represent a true statistical minimum strength if all variables are included.

5.5 RTV Adhesive Material Property Variation: The thermal expansion and elasticity properties of the RTV adhesive at low temperatures vary over a wide range depending on adhesive type and particular batch properties. There is even some evidence of temperature instability of the properties with variations in the volatiles making up the composition.

6.0 CONCLUSION

It is obvious that more work could be profitably expended in establishing the quantitative phenomena affecting the allowable low temperature silicon stress levels and additional development work in this area is strongly recommended. However, with careful material and surface finish controls, a marked increase in effective silicon/RTV adhesive allowable thermal stresses can be realized with a corresponding increase in design margins to prevent solar cell spalling at low temperatures. Emphasis will be placed upon this approach in selecting the sub-module silicon cells to be used on the Prototype Module.

TABLE A-1 DATA USED FOR REFINED STRESS ANALYSIS

REFINEMENT OF THERMAL STRESS EQUATION

$$f = N_o \left[\gamma (N_o)\right] \quad , \text{ Silicon Stress}$$

$$\gamma (N_o) = a + b/N_o \quad , \text{ Correction Factor}$$

where $a = 280.754$, $b = 1347.842$ } curvefit of Computer data

$N_o = tS$ Interlaminar Shear Load

$$S = E_T \int_T^{T_o} \alpha \, dt \quad \left(\begin{matrix}\text{RTV Bond} \\ \text{Material Parameter}\end{matrix}\right)$$

$f = [aSt + b]$ (Silicon Stress)

TEST DATA OF RTV PROPERTIES @ -173°C

Material	E_T (10^6psi)	α dt	t (in)	S (psi)	f (psi)
RTV-118	.173	.0827	.010	1430	5384
RTV-3145	.038	.0376	.020	143	2155*
RTV 511/577	.108	.0497	.010	537	2855
PR-1538	.038	.0267	.010	101	1380

NOTES:

* RTV-3145 is a highly volative adhesive with quite variable properties. The silicon cell used was also pre-stressed by flattening

\+ PR 1538 did not adhere to silicon cells due to primer failure

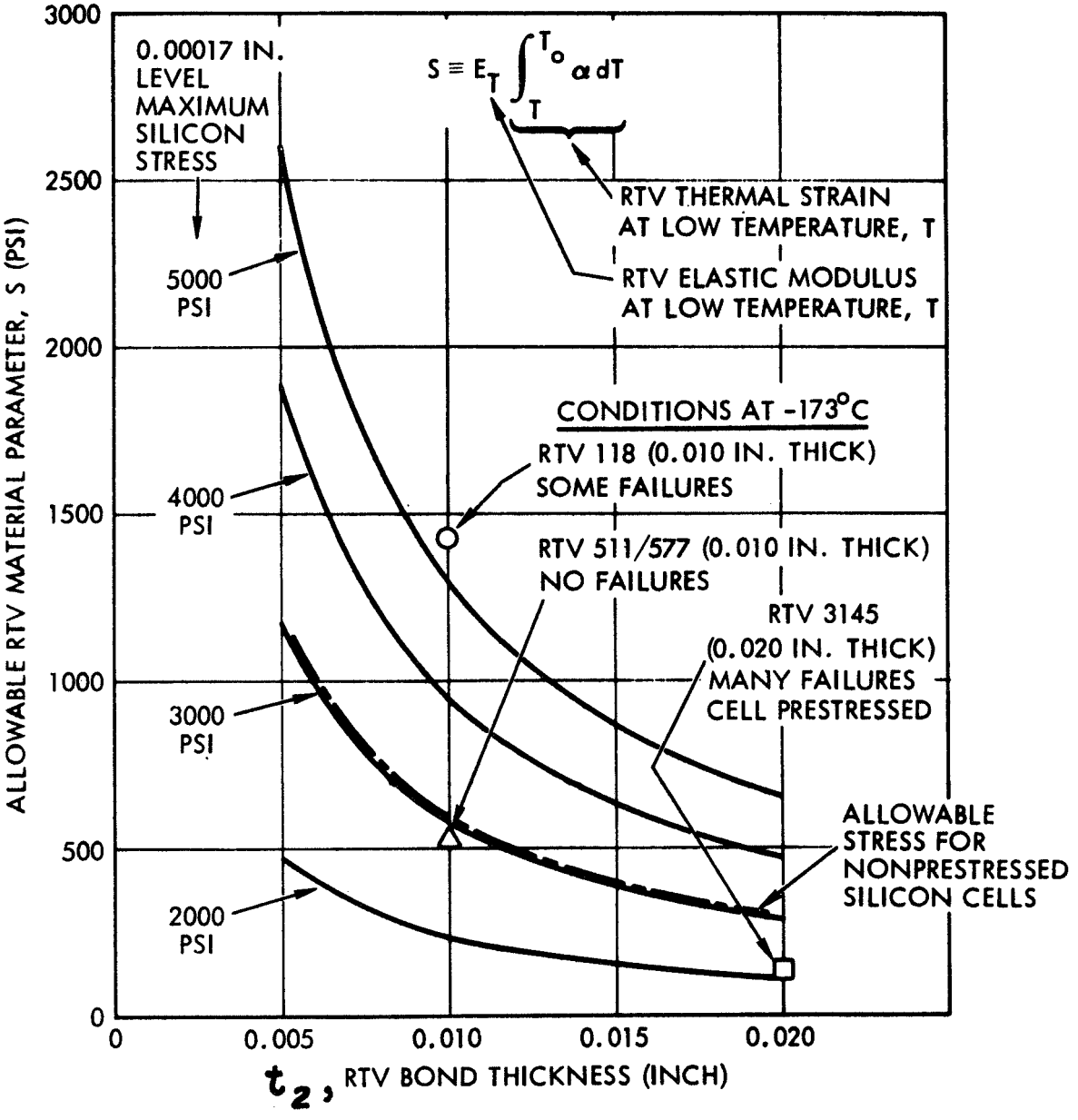


Figure A-1 Allowable RTV Bond Material Parameter, S vs. Silicon Stress and RTV Thickness

APPENDIX B

ELECTRICAL PERFORMANCE DATA

FOR

SEVEN STRINGS ON PROTOTYPE TEST MODULE

CHANNEL IDENTIFICATION

8 STANDARD CELL Isc
260.1 ∅ MA

4 ARRAY CURRENT UNCORRECTED
4823∅MA

3 ARRAY VOLTAGE UNCORRECTED
34.58∅ VOLTS

2. ARRAY CURRENT CORRECTED
485.2∅ MA

1. ARRAY VOLTAGE CORRECTED TO 28°C
34.15∅ VOC.

LUNAR BASE
ARRAY
P/N SK 120044
XENON FLASH TEST
P/N X311692
S/N 001

TEST TEMP 25°C
STD CELL SAS-CL-173
(261.1 MA)

INSULATION RESISTANCE AND ISOLATION BETWEEN STRINGS MEASURED USING TRIPLETT 630NA V.O.M ON Rx100K SCALE.

APR 28 1971 (32) T.S.

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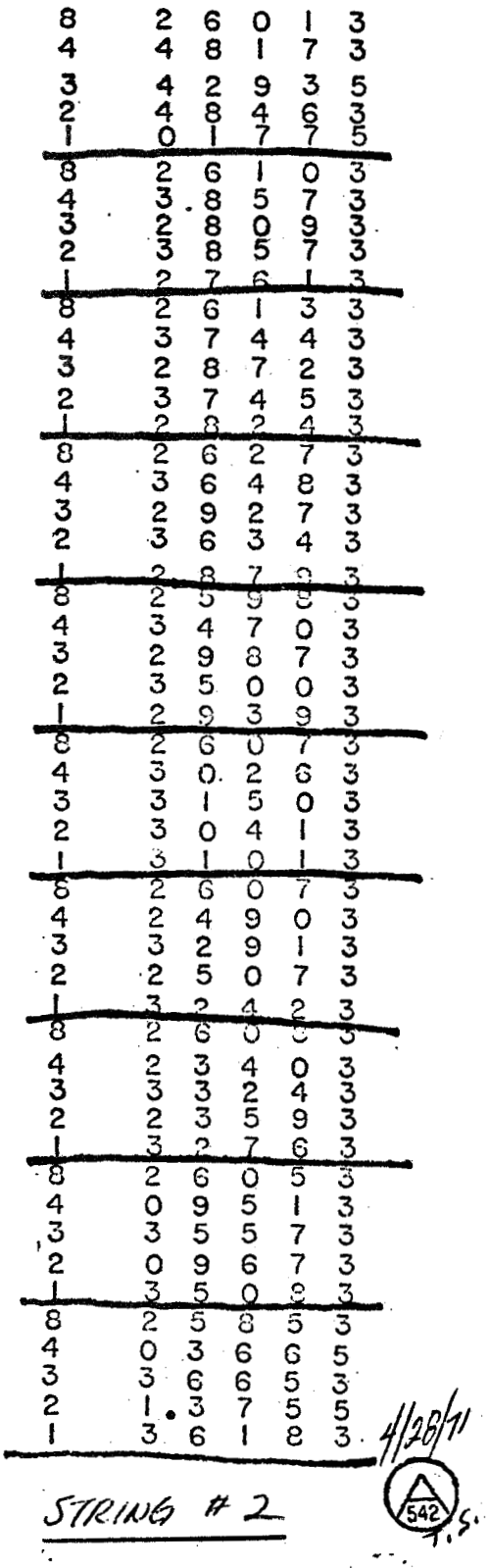

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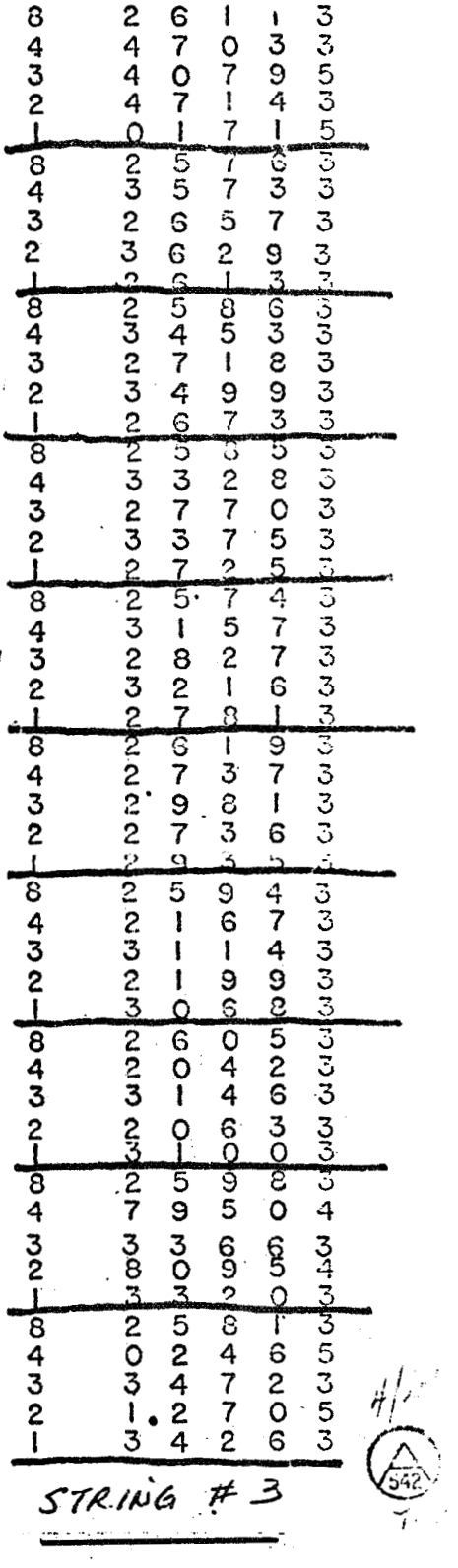

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1	3	1	1	5	3
8	2	5	8	1	3
4	7	6	2	2	4
3	3	3	3	3	3
2	7	8	0	9	4
1	3	3	3	8	3
8	2	6	0	2	3
4	0	1	0	6	5
3	3	4	8	5	3
2	1	0	8	5	5
1	3	4	4	1	3

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T.S.

STRING #4

8	2	6	0	0	3
4	4	8	2	6	3
3	3	4	9	3	5
2	4	8	5	7	3
1	0	7	2	9	5
8	2	5	7	8	3
4	3	4	9	3	3
3	2	6	3	7	3
2	3	5	4	8	3
1	2	5	9	2	3
8	2	5	8	0	3
4	3	3	6	0	3
3	2	6	9	7	3
2	3	4	1	4	3
1	2	6	5	2	3
8	2	5	7	9	3
4	3	2	2	6	3
3	2	7	4	9	3
2	3	2	8	0	3
1	2	7	0	3	3
8	2	6	2	0	3
4	3	1	5	4	3
3	2	8	0	5	3
2	3	1	5	6	3
1	2	7	6	0	3
8	2	6	1	1	3
4	2	6	2	8	3
3	2	9	5	8	3
2	2	6	3	6	3
1	2	9	1	2	3
8	2	5	8	8	3
4	2	0	6	5	3
3	3	0	9	0	3
2	2	1	0	0	3
1	3	0	4	5	3
8	2	5	8	1	3
4	1	9	0	9	3
3	3	1	2	1	3
2	1	9	4	5	3
1	3	0	7	5	3
8	2	5	7	8	3
4	7	1	3	4	4
3	3	3	4	0	3
2	7	3	1	6	4
1	3	2	9	6	3
8	2	5	8	7	3
4	0	4	3	0	5
3	3	4	4	0	3
2	1	3	6	7	5
1	3	3	9	7	3

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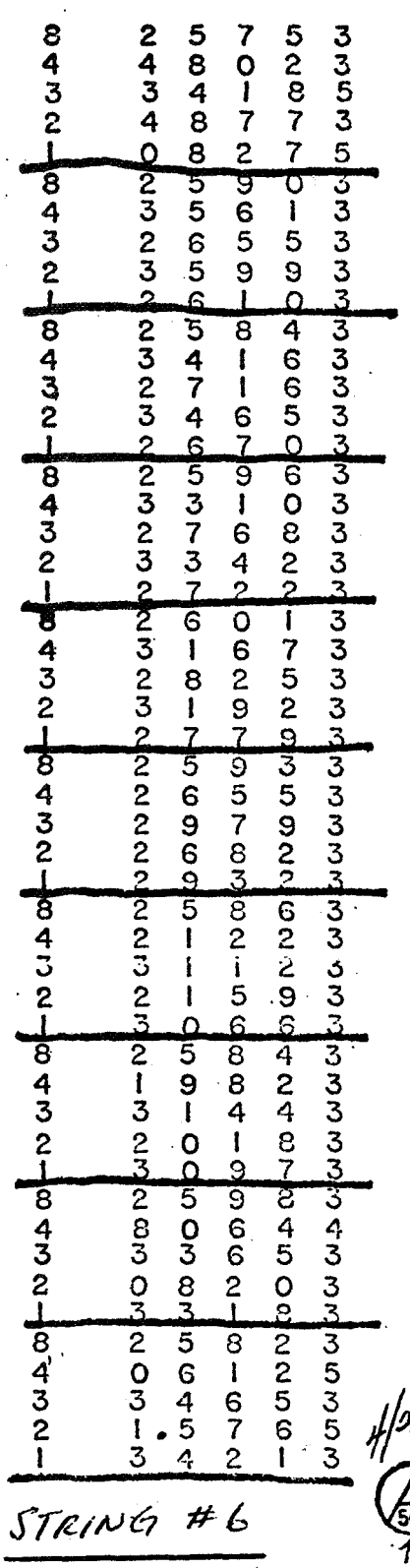
T.S.

STRING #5



STRING #6

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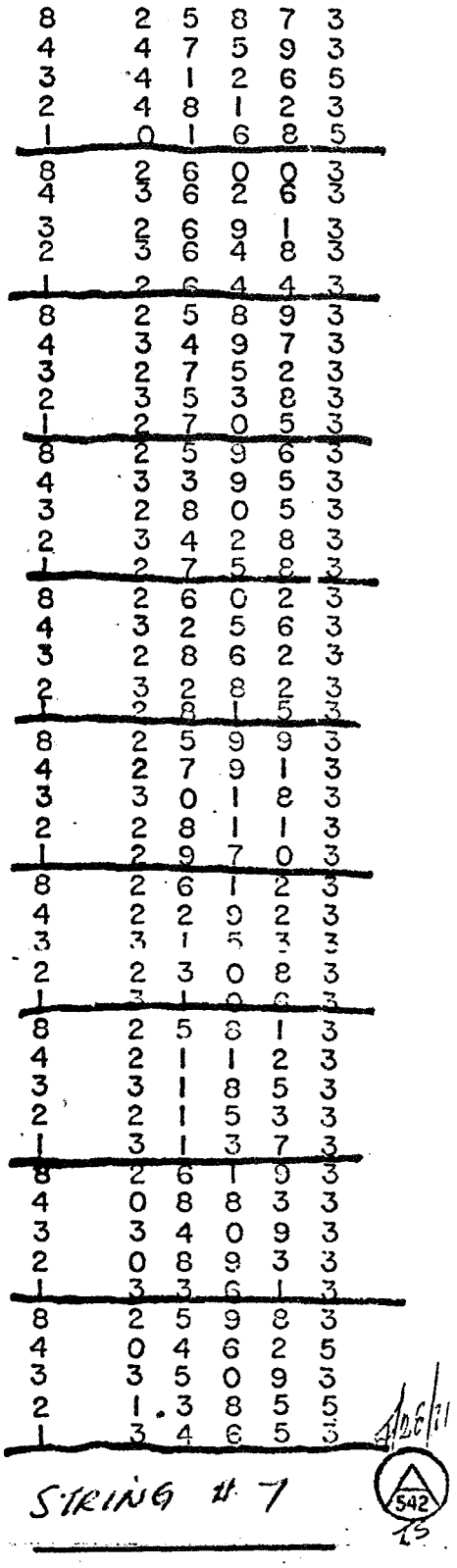
T.C.



STRING #7

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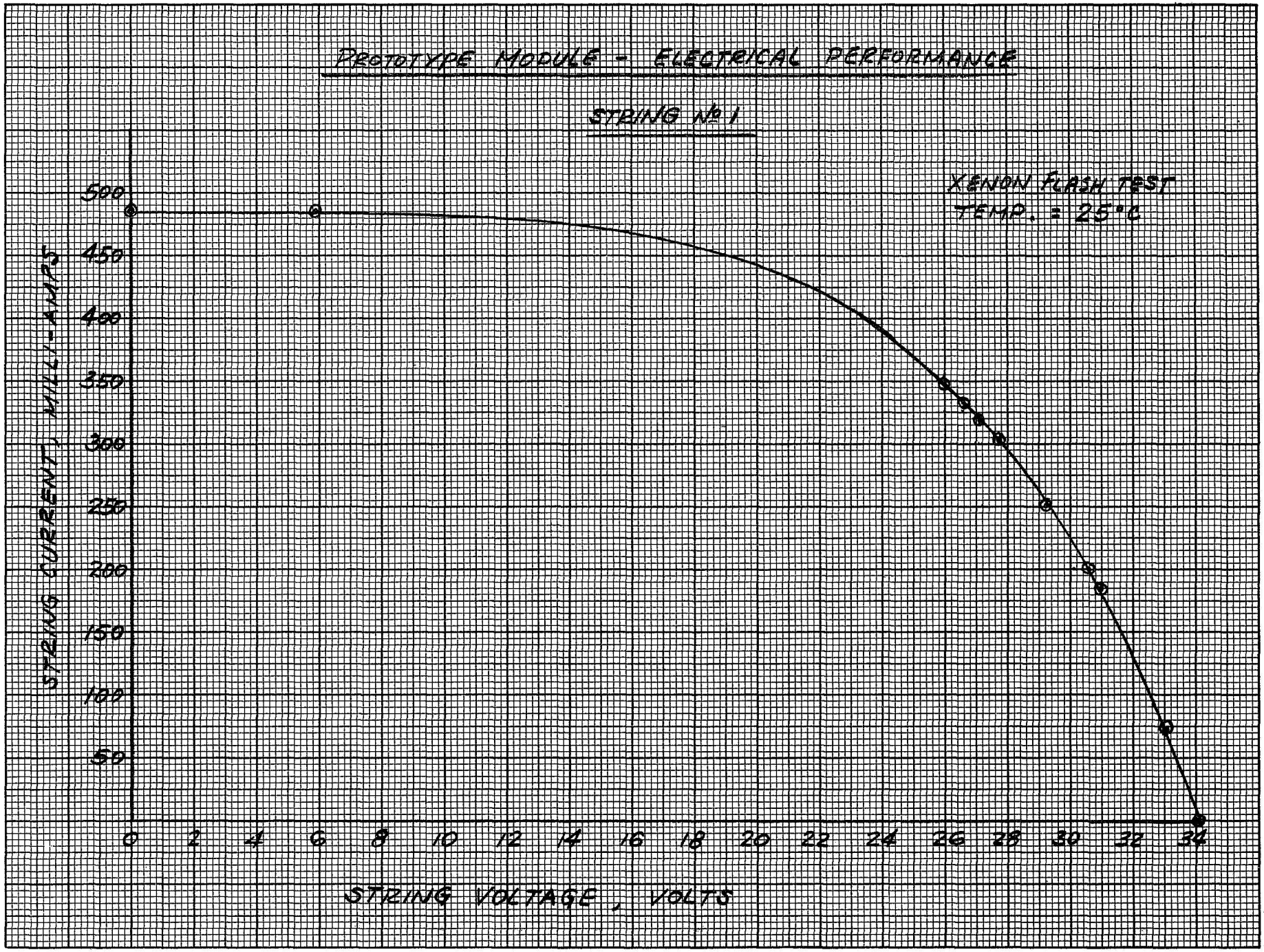
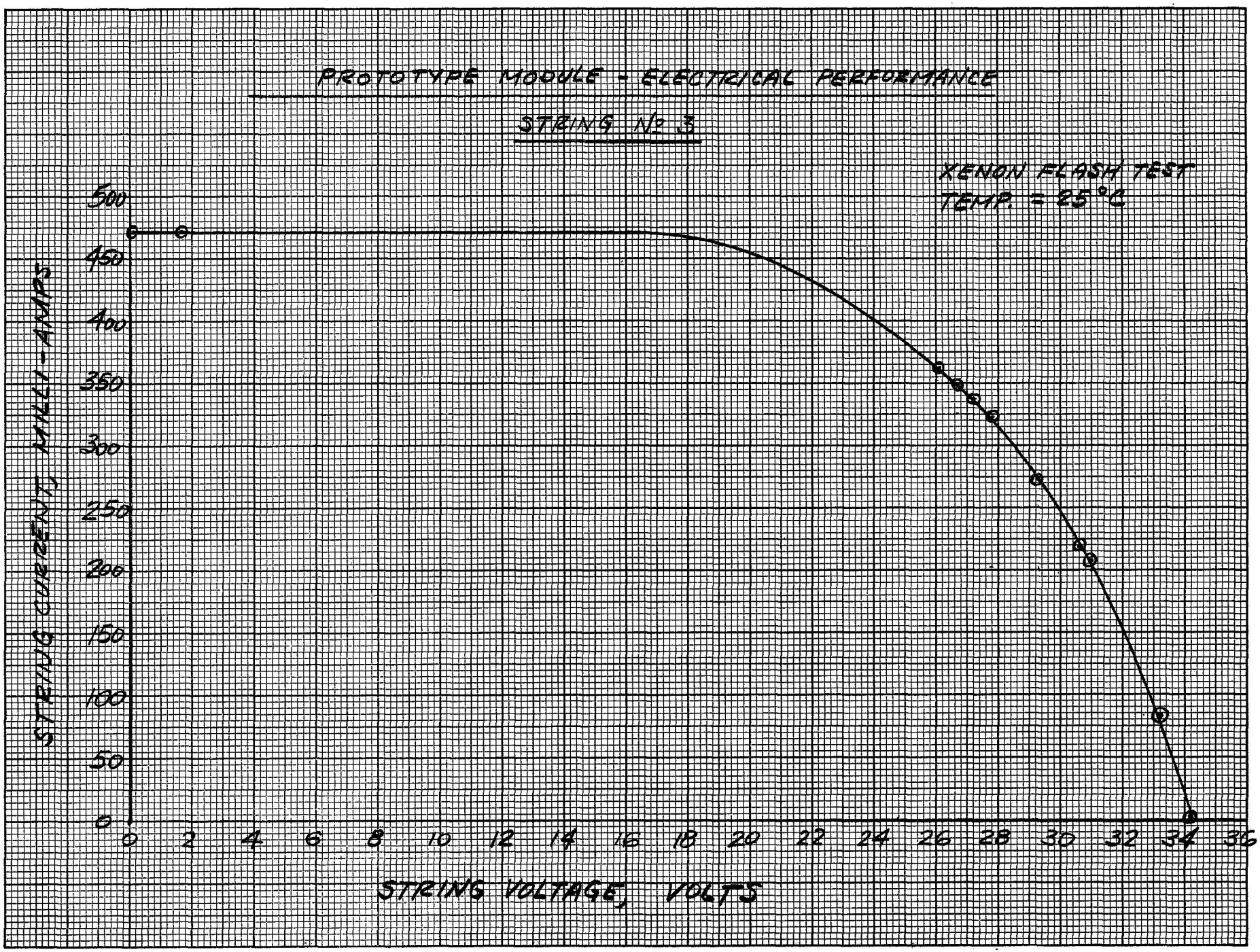
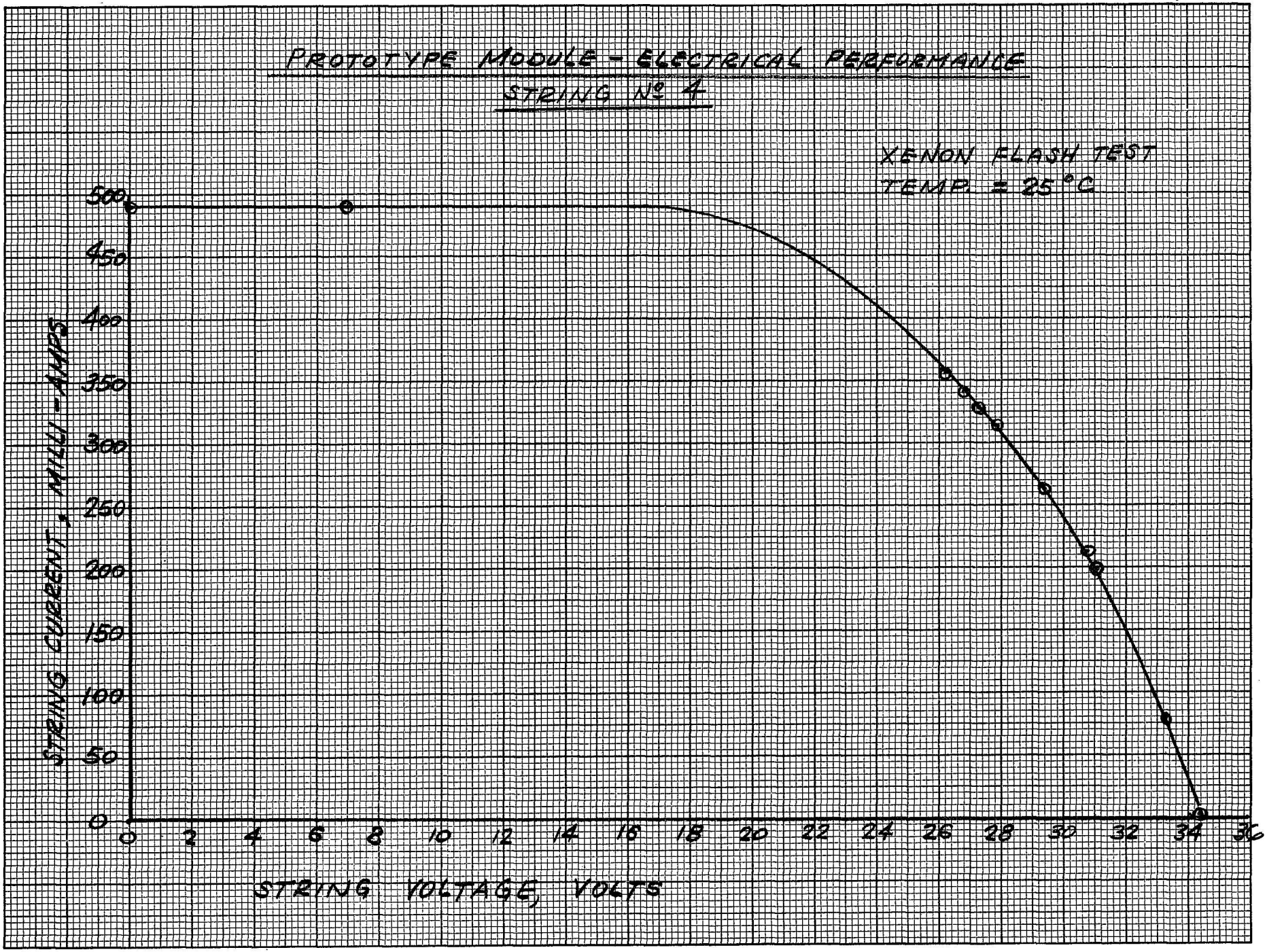

PROTOTYPE MODULE - ELECTRICAL PERFORMANCE
STRING № 1
XENON FLASH TEST
TEMP. = 25°C
STRING CURRENT, MILLI-AMPS
500
450
400
350
300
250
200
150
100
50
0
2
4
6
8
10
12
14
16
18
20
22
24
26
28
30
32
34
STRING VOLTAGE, VOLTS

PROTOTYPE MODULE - ELECTRICAL PERFORMANCE
STRING #2
Xenon Flash Test
Temp. = 25°C
STRING CURRENT, MILLI-AMPS
STRING VOLTAGE, VOLTS
0
50
100
150
200
250
300
350
400
450
500
0
2
4
6
8
10
12
14
16
18
20
22
24
26
28
30
32
34
36


PROTOTYPE MODULE - ELECTRICAL PERFORMANCE
STRING NO. 3
XENON FLASH TEST
TEMP. = 25°C
500
450
400
350
300
250
200
150
100
50
0
0
2
4
6
8
10
12
14
16
18
20
22
24
26
28
30
32
34
36
STRING VOLTAGE, VOLTS


PROTOTYPE MODULE - ELECTRICAL PERFORMANCE
STRING Nº 4
XENON FLASH TEST
TEMP. = 25 °C
STRING CURRENT, MILLI-AMPS
500
450
400
350
300
250
200
150
100
50
0
0 2 4 6 8 10 12 14 16 18 20 22 24 26 28 30 32 34 36
STRING VOLTAGE, VOLTS

PROTOTYPE MODULE ELECTRICAL PERFORMANCE
STRING #15
XENON FLASH TEST
TEMP. = 25°C
STRING VOLTAGE, VOLTS
STRING CURRENT, MILLI-AMPS
0
2
4
6
8
10
12
14
16
18
20
22
24
26
28
30
32
34
36
500
450
400
350
300
250
200
150
100
50

Piezotube Module - Electrical Feedthrough
2 Strings No. 6
Xenon Flash Test
Temp. = 25°C
STRING CURRENT, milli-amps
STRING VOLTS, volts

Typical Test Curve
Temp. = 25°C
Stress Voltage, Volts
Steady Current, milli-Amps